AP
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Date: 3/15/06

Lisa D. Jones
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Samuel D. Naffziger, et al.
Serial No.	:	10/648,570
Filing Date	:	August 26, 2003
Art Unit	:	2817
Examiner:	:	Michael B. Shingleton
Confirmation No.	:	4101
Title	:	**SYSTEM AND METHOD TO ADJUST VOLTAGE**

Mail Stop APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF

Sir:

Following the Notice of Appeal filed January 26, 2006, Appellant presents this Appeal Brief.

1. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company L.P.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

3. STATUS OF CLAIMS

Claims 9-11, 18 and 27-30 have been allowed. Claims 1-2, 4-8, 13-17, 19-26 and 31 have been cancelled. Claims 3 and 12 stand rejected and are appealed.

4. STATUS OF AMENDMENTS

Claims 1-2, 4-8, 13-17, 19-26 and 31 were cancelled in an Amendment After Final and Response to Office Action that was filed on November 28, 2005. Claims 3, 9-12, 18, and 27 were also amended in the response filed on November 28, 2005. All of these amendments were entered for purposes of appeal.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

a. Claim 3

In the context of FIG. 4, claim 3 recites a system (150) that comprises a frequency generator (156) that provides a clock signal (*e.g.*, CLK_{OUT}) having a frequency that varies based on an operating voltage (*e.g.*, V_{SUPPLY}). Present application, at page 11, lines 23-25 (as amended in Response dated July 11, 2005. Present application, at page 11, lines 10-12. A controller (152) provides a control signal to adjust the operating voltage based on adjustments to the frequency of the clock signal. Present application, at page 11, lines 22-24. The controller (152) provides the control signal based on a number of cycles for the clock signal (*e.g.*, CLK_{OUT}) relative to a number of cycles for a second signal (*e.g.*, CLK_{IN}) over a cycle time that encompasses plural cycles associated with the clock signal and the second signal.

Present application, at page 12, lines 18-24, and at page 13, lines 12-18. The second signal (*e.g.*, CLK_{IN}) has a substantially fixed frequency, wherein the clock signal (*e.g.*, CLK_{OUT}) defines a variable clock signal and the second signal defines a signal having a substantially fixed maximum frequency for the clock signal. Present application, at page 11, lines 15-24.

b. Claim 12

In the context of FIG. 4, claim 12 recites a system (150) that comprises a frequency generator that provides a clock signal (*e.g.*, CLK_{OUT}) having a frequency that varies based on an operating voltage (*e.g.*, V_{SUPPLY}). Present application, at page 11, lines 23-25 (as amended in Response dated July 11, 2005. Present application, at page 11, lines 10-12. A controller (152) provides a control signal to adjust the operating voltage (*e.g.*, V_{SUPPLY}) based on adjustments to the frequency of the clock signal (*e.g.*, CLK_{OUT}). Present application, at page 11, lines 22-24. A second frequency generator provides a second signal having a substantially fixed frequency corresponding to a desired maximum frequency for the clock signal (*e.g.*, CLK_{OUT}). Present application, at page 11, lines 15-24.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

i. Whether claim 3 is anticipated by U.S. Patent No. 5,416,446 to Holler Jr. et al.

ii. Whether claim 12 is anticipated by U.S. Patent No. 5,416,446 to Holler Jr. et al.

7. ARGUMENT

A. The rejection of independent claims 3 and 12 as being anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 5,416,446 to Holler Jr. et al. is improper because Holler Jr. et al. does not teach, explicitly or inherently, the recitations of claims 3 and 12.

The Court of Appeals for the Federal Circuit has held that, "to anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or

inherently." In re Schreiber, 128 F. 3d 1473, 44 U.S.P.Q.2d 1429 (Fed. Cir. 1997). The Court of Appeals for the Federal Circuit also mandates that an anticipatory reference must enable an ordinarily skilled artisan to make and use claimed invention. In re Donahue, 766 F.2d 531, 533 (Fed. Cir. 1985). The Court of Appeals for the Federal Circuit elaborated on this standard in In re Elsner, 381 F.3d 1125, 1128, 72 U.S.P.Q.2d 1038 (Fed. Cir. 2004), stating:

> Prior art under § 102(b) must sufficiently describe a claimed invention to have placed the public in possession of that invention. The proper test of a publication as a § 102(b) bar is "whether one skilled in the art to which the invention pertains could take the description of the invention in the printed publication and combine it with his own knowledge of the particular art and from this combination be put in possession of the invention on which a patent is sought." In re Elsner, *supra.*, *citing* In re Donohue, 766 F.2d 531, 533 (Fed. Cir. 1985) and In re Samour, 571 F.2d 559, 562 (CCPA 1978).

i. The rejection of claim 3 under §102(b)

Claim 3 stands rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,416,446 to Holler Jr. et al. (hereinafter "Holler"). Appellant respectfully requests that this rejection be withdrawn for the following reasons.

In contrast to the position asserted in a Final Office Action, dated October 5, 2005 (hereinafter the "Final Office Action"), Holler fails to teach or suggest the claimed relationship between the clock signal and a second signal; namely, that the second signal has a substantially fixed frequency that defines a maximum frequency for the clock signal, as recited in claim 3. The Final Office Action supports Applicant's position since the Final Office Action fails to cite or reference any teaching in Holler corresponding to the claimed interrelationship between the clock signal and a second signal. In discussing claim 2 (from which claim 3 originally depended and which has been incorporated into present claim 3), the Final Office Action states that "the fixed frequency is the second signal from element 105...

and the signal at the output of element 102 would be the first signal." Final Office Action, at Page 3, lines 6-9. The "first signal" of claim 3 identified in the Final Office Action corresponds to the "clock signal" and appropriate amendment has been made by prior amendment to claim 3 to correct this typographical error.

Holler teaches that a counter 108 counts the number of cycles of the ring oscillator 102 during a known interval, which is a function of the crystal 106 connected to the crystal oscillator 105. Holler, at Col. 3, lines 62-66. A comparator 108 inspects the counter value to determine whether the frequency of the ring oscillator 102 should be changed. Holler, at Col. 4, lines 1-4. Moreover, in the circuitry of Holler, the maximum frequency of the ring oscillator 102 output is established by the impedance of the delay elements 201, 202 and 203 and properties of a binary current tree 101. In particular, a minimum frequency of the ring oscillator 102 is provided when transistors 222 and 223 are on (See, *e.g.*, Holler at Col. 2, line 67, through Col. 3, line 2). By contrast, a maximum frequency for the ring oscillator 102 is provided when the BIG, MED and SML banks 204, 207, 210, 213, 216 and 219 are fully activated. The transistors in the banks are controlled by the ring frequency registers 111 according to signals generated by the comparator 110. Holler, at Col. 3, lines 31-33. The circuitry disclosed in Holler thus operate in sharp contrast to in claim 3, which recites the use of the second signal to define a signal having a substantially fixed maximum frequency for the clock signal.

Applicant submits that no knowledge of one of ordinary skill in the art would be able to make up for the above-mentioned deficiencies in Holler so as support that the public possessed the invention on which a patent is sought. *See* In re Elsner, *supra.* Therefore, the description in Holler Jr. et al. is inadequate as a statutory bar to patentability of claim 3 under 35 U.S.C. §102(b). Accordingly, reversal of the rejection of claim 3 is respectfully requested.

ii. **The rejection of claim 12 under §102(b)**

Regarding claim 12, the Office Action states, "[e]lement 105 would be the second frequency generator of claims like claim 12." Office Action dated October 5, 2005, at Page 3, lines 7-8. However, Holler teaches that a counter 108 counts the number of cycles of the ring oscillator 102 during a known interval, which is a function of the crystal 106 connected to the crystal oscillator 105. Holler, at Col. 3, lines 62-66. The comparator 108 inspects the counter value to determine whether the frequency of the ring oscillator 102 should be changed. Holler, at Col. 4, lines 1-4.

Additionally, the circuitry of Holler establishes the maximum frequency of the ring oscillator 102 output based on the impedance of the delay elements 201, 202 and 203 and properties of a binary current tree 101. In particular, a minimum frequency of the ring oscillator 102 is provided when transistors 222 and 223 are on (See, *e.g.*, Holler at Col. 2, line 67, through Col. 3, line 2). By contrast, a maximum frequency for the ring oscillator 102 is provided when the BIG, MED and SML banks 204, 207, 210, 213, 216 and 219 are fully activated. The transistors in the banks are controlled by the ring frequency registers 111 according to signals generated by the comparator 110. Holler, at Col. 3, lines 31-33. The system disclosed in Holler thus fails to teach a second frequency generator provides a second signal having a substantially fixed frequency corresponding to a desired maximum frequency for the clock signal, as recited in claim 12.

Applicant submits that no knowledge of one of ordinary skill in the art would be able to make up for the above-mentioned deficiencies in Holler so as support that the public possessed the invention on which a patent is sought. *See* In re Elsner, *supra.* Therefore, the description in Holler Jr. et al. is inadequate as a statutory bar to patentability of claim 12

under 35 U.S.C. §102(b). Accordingly, reversal of the rejection of claim 12 is respectfully requested.

B. Conclusion

In view of the foregoing, Appellant respectfully submits that claims 3 and 12 are allowable. Reversal of the rejection is respectfully requested.

8. APPENDICES

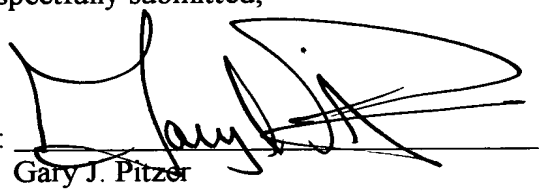
Appendix A submitted herewith is a Claims Appendix containing a copy of the claims on appeal.

Appendix B submitted herewith is an Evidence Appendix.

Appendix C submitted herewith is a Related Proceedings Appendix.

If any fees are due in connection with filing of this document or at any time during this appeal, including for any extensions of time, please charge any deficiency or credit any overpayment in the fees to Deposit Account No. 08-2025.

Respectfully submitted,

By: 

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Appendix A

CLAIMS APPENDIX

3. A system comprising:

a frequency generator that provides a clock signal having a frequency that varies based on an operating voltage; and

a controller that provides a control signal to adjust the operating voltage based on adjustments to the frequency of the clock signal, wherein the controller provides the control signal based on a number of cycles for the clock signal relative to a number of cycles for a second signal over a cycle time that encompasses plural cycles associated with the clock signal and the second signal, the second signal having a substantially fixed frequency, wherein the clock signal defines a variable clock signal and the second signal defines a signal having a substantially fixed maximum frequency for the clock signal.

9. A system comprising:

a frequency generator that provides a clock signal having a frequency that varies based on an operating voltage;

a controller that provides a control signal to adjust the operating voltage based on adjustments to the frequency of the clock signal;

a comparator operative to ascertain an indication of throttle events associated with the frequency generator implementing changes to the frequency of the clock signal, the controller providing the control signal based on the indication of throttle events; and

first and second counters, the first counter being operative to count a number cycles associated with the clock signal, the second counter being operative to count a number cycles associated with a second signal having a substantially fixed frequency, the comparator ascertaining the indication of throttle events based on the relative number of cycles counted by the first and second counters.

10. A system comprising:

a frequency generator that provides a clock signal having a frequency that varies based on an operating voltage;

a controller that provides a control signal to adjust the operating voltage based on adjustments to the frequency of the clock signal; and

first and second counters, the first counter being operative to count a number cycles associated with the clock signal, the second counter being operative to count a number cycles associated with a second signal having a substantially fixed frequency, the controller providing the control signal based on the relative number of cycles counted by the first and second counters.

11. The system of claim 10, wherein the relative number of cycles indicated by the first and second counters corresponds to an average indication of a number of changes implemented by the frequency generator to the frequency of the clock signal.

12. A system comprising:

a frequency generator that provides a clock signal having a frequency that varies based on an operating voltage;

a controller that provides a control signal to adjust the operating voltage based on adjustments to the frequency of the clock signal; and

a second frequency generator that provides a second signal having a substantially fixed frequency corresponding to a desired maximum frequency for the clock signal.

18. A system to adjust voltage, comprising:

means for providing an indication of voltage induced throttle events for an integrated circuit; and

means for controlling a supply voltage of the integrated circuit based on the indication of throttle events;

means for determining a number of cycles for the clock signal relative to a number of cycles for a second signal having a substantially fixed frequency, the determined number of cycles providing an indication of throttle events associated with changes in a frequency of the clock signal, wherein the means for determining further comprising:

means for counting cycles of the clock signal; and

means for counting cycles of the second signal,

the means for controlling adjusting the supply voltage of the integrated circuit based on a relative number of cycles counted by each of the means for counting cycles.

27. A method comprising:

determining whether adjustments to an operating frequency of an integrated circuit are within expected operating parameters based on adjustments made to the operating frequency performed over a cycle time that includes a plurality of cycles at the operating frequency;

adjusting a supply voltage based on the determination;

counting a number of cycles associated with a first reference signal having a substantially fixed frequency at a maximum operating frequency;

counting a number of cycles associated with a second reference signal provided at the operating frequency that varies based on the supply voltage; and

comparing the number of cycles associated with the first reference signal relative to the number of cycles associated with the second reference signal, the adjustment to the supply voltage being made based on the comparison.

28. The method of claim 27, further comprising ascertaining an indication of throttle events associated with adjustments to the frequency of the second reference signal based on the comparison, the adjustment to the supply voltage being made based on the indication of throttle events.

29. The method of claim 28, wherein the adjustment to the supply voltage are made based on comparing the indication of throttle events relative to at least one threshold, the adjustment to the supply voltage being made based on the comparison.

30. The method of claim 29, further comprising programming the at least one threshold to define operating categories for adjusting the supply voltage.

Appendix B

EVIDENCE APPENDIX

There was no evidence relied upon in this brief that was submitted under 37 C.F.R. §§1.130-1.132, or otherwise submitted and entered into the record by the Examiner.

Appendix C

RELATED PROCEEDINGS APPENDIX

There are no related appeals, interferences, or judicial procedures under 37 C.F.R. §41.37(1)(c)(ii).

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PATENT APPLICATION

ATTORNEY DOCKET NO. 200208858-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Samuel D. Naffziger, et al.

Confirmation No.: 4101

Application No.: 10/648,570

Examiner: M. B. Shingleton

Filing Date: August 23, 2003

Group Art Unit: 2817

Title: SYSTEM AND METHOD TO ADJUST VOLTAGE

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **01/26/2006**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: **March 15, 2006**

OR

( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number_____ on _____

Number of pages:

Typed Name: **Lisa D. Jones**

Signature: Lisa D. Jones

Respectfully submitted,

Samuel D. Naffziger, et al.

By _____

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